IN THE CLAIMS

Claims 1-32 (Canceled)

33. (Original) An apparatus for identifying defects in an integrated circuit, comprising:

a generator for generating a set of vectors for applying to a device under test;

a measurer for measuring a current signature delta value of the device under test; and

a comparing means for comparing the current signature delta value to an experimental threshold current signature delta value to determine whether the current signature delta value is greater than the threshold current signature delta value.

34. (Original) The apparatus according to claim 33, wherein the measurer measures the experimental threshold current signature delta value for the statistically valid number of acceptable integrated circuits by:

applying a set of vectors to the statistically valid number of acceptable integrated circuits;

formulating a threshold base current signature for the statistically valid number of acceptable integrated circuits from the set of measured vectors;

administering a voltage stress for a time period to the statistically valid number of acceptable integrated circuits;

applying the set of vectors to the statistically valid number of acceptable integrated circuits;

formulating a threshold post-stress current signature for the statistically valid number of acceptable integrated circuits from the set of measured vectors; and

comparing the threshold base current signature for the statistically valid number of acceptable integrated circuits to the threshold post-stress current signatures for the statistically valid number of acceptable integrated circuits to determine a threshold current signature delta value corresponding to an acceptable integrated circuit.

35. (Original) The apparatus according to claim 33, further comprising a computer for computing the experimental threshold current signature delta value.

36. (Original) The apparatus according to claim 33, wherein the generator generates a set of measured vectors from the set of vectors for applying to the device under test.

37. (Original) The apparatus according to claim 35, wherein the measurer measures the current signature delta value of the device under test by:

applying a set of vectors to the device under test;

formulating a base current signature for the device under test from the set of measured vectors;

administering a voltage stress for a time period to the device under test;

applying the set of vectors to the device under test;

formulating a threshold post-stress current signature for the device under test from the set of measured vectors;

comparing the base current signature for the device under test to the post-stress current signatures for the device under test to determine a the current signature delta value for the device under test.

38. (Original) The apparatus according to claim 36, wherein the measurer measures the current signature delta value of the device under test by:

applying a set of vectors to the device under test;

formulating a base current signature for the device under test from the set of measured vectors;

administering a voltage stress for a time period to the device under test;

applying the set of vectors to the device under test;

formulating a threshold post-stress current signature for the device under test from the set of measured vectors; and

comparing the base current signature for the device under test to the post-stress current signatures for the device under test to determine a the current signature delta value for the device under test.

39. (Original) The apparatus according to claim 37, wherein the threshold current signature delta value generated by the generator is equivalent to a largest difference between the post-voltage stress current signature and the base current signature of the statistically valid number of acceptable integrated circuits.

40. (Original) The apparatus according to claim 38, wherein the threshold current signature delta value generated by the generator is equivalent to a largest difference between the post-voltage stress current signature and the base current signature of the statistically valid number of acceptable integrated circuits.

41. (Original) The apparatus according to claim 39, wherein the current signature delta value for the device under test is a difference between the post-voltage stress current signature and the base current signature of the device under test.

42. (Original) The apparatus according to claim 41, wherein the generator generates the set of vectors for applying to a statistically valid number of acceptable integrated circuits; and the measurer measures the experimental threshold current signature delta value of the statistically valid number of acceptable integrated circuits.